

Compal Confidential

CIUYA/YB

Alpine I/O Board Schematic Document














LS-E541P

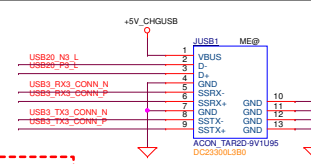
2017-01-05

REV:1.0

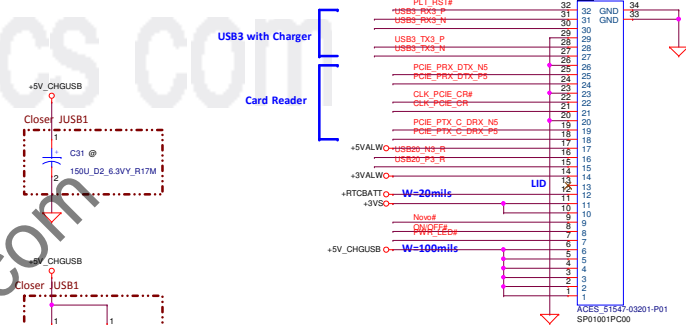
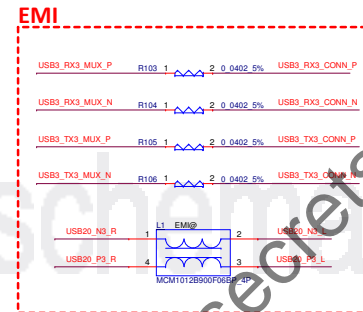
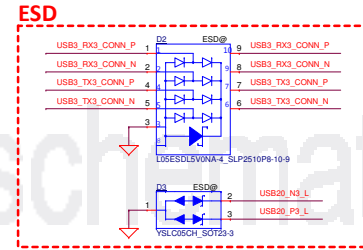
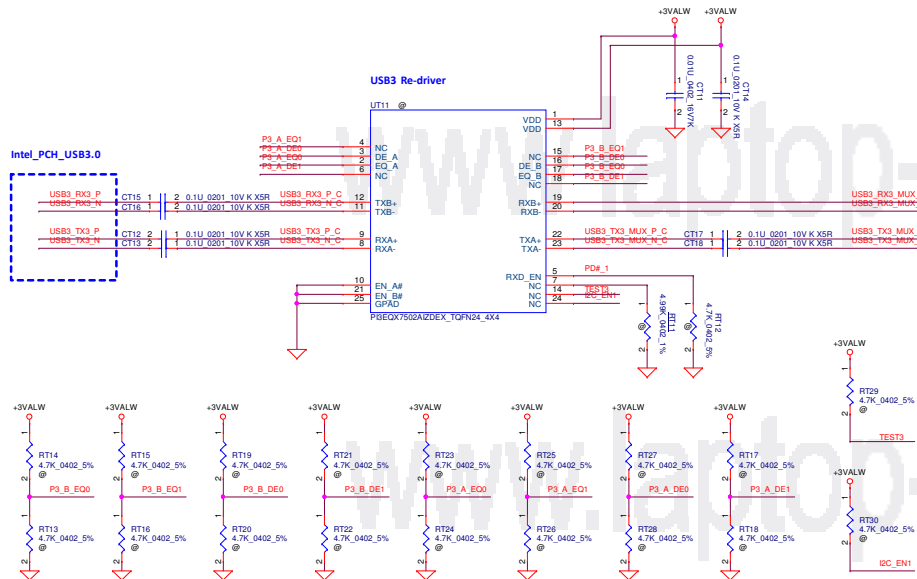
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Issued Date		2017/01/05		Title	
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				Custom	LS-E541P
				Date:	Thursday, January 05, 2017
				Sheet	1 of 3

USB3.0 Port

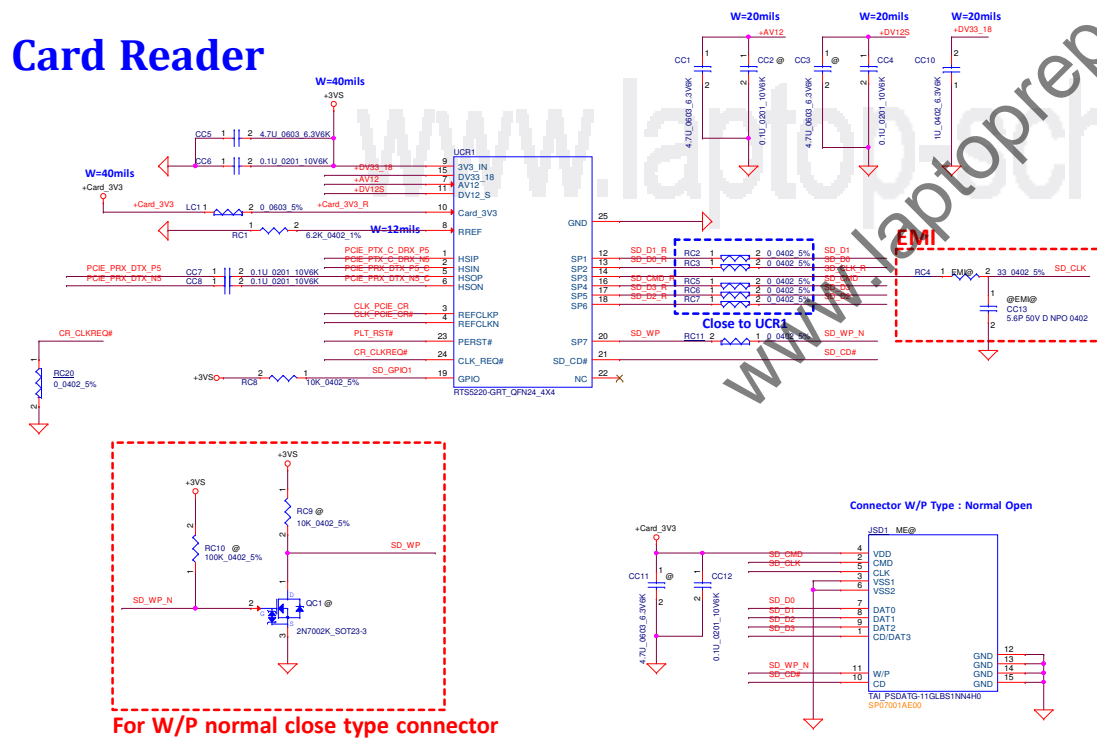
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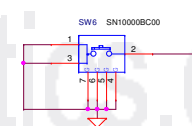
I/O CONN



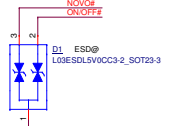
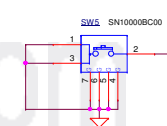
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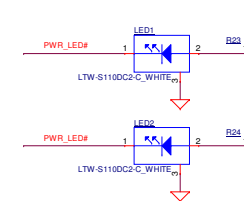
PWR Button



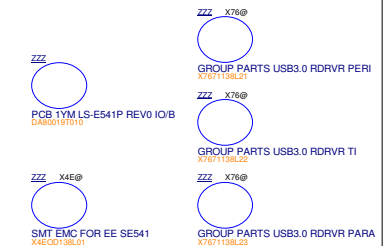
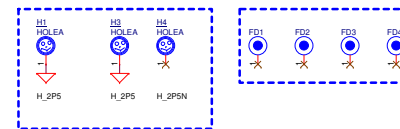
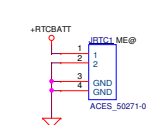
Novo Button



Power LED (White)



RTC CONN



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			Doc Number	1.0
			IO/SD/USB CONN	
			LS-ES41P	
Date: Monday, January 09, 2017				

Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	USB3.0 EA test result	2	Stuff RT13, RT20, RT24, RT28	09/12	EVT to DVT
2	DFX Request (Factory Rule)	2	Remove R101 and R102 (Remove 0-ohm path, remain choke)	11/09	DVT to PVT
3	ME Request for PWR Button (Fine Tune LED Resistor)	2	R23, R24 change to 976 ohm (Original: 412 ohm)	11/17	DVT to PVT
4	ME Request for PWR Button (Fine Tune LED Resistor)	2	Pop R24 and LED2	11/21	DVT to PVT
5	TI Re-Driver Resistor Fine-Tune	2	Un-Pop RT19, Mount RT20	11/28	DVT to PVT
6	DFX Request (Factory Rule)	2	Remove Choke L2, L3 and R103, R104, R105, R106 Co-Layout Path	01/05	PVT to Pre-MP
7					
8					
9					
10					
11					
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				HW PIR	
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